```
     FILE 'CAPLUS' ENTERED AT 18:25:02 ON 10 AUG 2003
L5       164007 S QUARTZ
L6          155 S L5 AND JIG
L7            3 S L6 AND (PTFE OR TFE OR ?FLUORO?)
L8           76 S L5 AND (RADIUS OF CURVATURE?)
L9            1 S L8 AND ?FLUORO?

     FILE 'USPATFULL, USPAT2' ENTERED AT 18:28:29 ON 10 AUG 2003
L10         278 FILE USPATFULL
L11          14 FILE USPAT2
     TOTAL FOR ALL FILES
L12         292 S L7
L13          10 FILE USPATFULL
L14           3 FILE USPAT2
     TOTAL FOR ALL FILES
L15          13 S L12 AND (RADIUS OF CURVATURE?)
L16          13 FOCUS L15 1-

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=>
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L16 ANSWER 1 OF 13 USPATFULL on STN
AN 2002:198422 USPATFULL
TI **Fluororesin**-coated **quartz** glass **jig** and method for producing the same
IN Inaki, Kyoichi, Tokorozawa-shi, JAPAN
Araki, Itsuo, Kikuchi-shi, JAPAN
PI US 2002106518 A1 20020808
AI US 2001-6827 A1 20011204 (10)
PRAI JP 2000-369534 20001205
DT Utility
FS APPLICATION
LREP LAW OFFICE OF ANDREW L. TIAJOLOFF, C/O ROBIN BLECKER & DALEY, 330 MADISON AVENUE, NEW YORK, NY, 10017
CLMN Number of Claims: 15
ECL Exemplary Claim: 1
DRWN No Drawings
LN.CNT 308
CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AB An object of the present invention is to provide a **fluororesin**-coated **quartz** glass **jig** free from peeling off of **fluororesin** coating on using hydrofluoric acid or from generating particles due to the etching of **quartz** glass, while yet preventing the generation of chipping by relaxing the impact imposed on the **quartz** glass by silicon wafers. It also is an object of the present invention to provide a production method of the **fluororesin**-coated **quartz** glass **jig**. The object above is achieved by a **fluororesin**-coated **quartz** glass **jig** the surface thereof is wholly covered with a pinhole-free **fluororesin** coating, and by a method for producing the same.
INCL INCLM: 428/421.000
NCL NCLM: 428/421.000
IC [7]
ICM: B32B027-00

CHEMICAL ABSTRACTS INDEXING COPYRIGHT 2003 ACS on STN

	PATENT	KIND	DATE
OS CA 137:9680	* EP 1213269	A1	20020612

* CA Indexing for this record included
CC 57-1 (Ceramics)
Section cross-reference(s): 76
ST quartz glass silicon wafer cleaning fluororesin coating; semiconductor device fabrication silicon wafer cleaning
IT Coating materials
(acid-resistant; manuf. of acid-resistant fluororesin-coated quartz glass jig for use in cleaning silicon wafers)
IT Semiconductor device fabrication
(cleaning silicon wafers; manuf. of acid-resistant fluororesin-coated quartz glass jig for use in cleaning silicon wafers)
IT Fluoropolymers, uses
(fluororesin coating; manuf. of acid-resistant fluororesin-coated quartz glass jig for use in cleaning silicon wafers)
IT Etching
(of quartz glass; manuf. of acid-resistant fluororesin-coated quartz glass jig for use in cleaning silicon wafers)
IT Fluoropolymers, uses
(perfluoroalkyl vinyl ether derivs., glass coating with; manuf. of acid-resistant fluororesin-coated quartz glass jig for use in cleaning silicon wafers)
IT 7631-86-9, Silicon dioxide, uses

(cryst. powder; manuf. of acid-resistant fluororesin-coated quartz glass jig for use in cleaning silicon wafers)
IT 75-02-5D, Vinyl fluoride, resin 75-38-7D, Vinylidene difluoride, resin 79-38-9D, Chlorotrifluoroethylene, resin 25038-71-5, Ethylenetetrafluoroethylene copolymer 25101-45-5, Ethylenechlorotrifluoroethylene copolymer 27029-05-6, Perfluoroethylenepropylene copolymer
(glass coating with; manuf. of acid-resistant fluororesin-coated quartz glass jig for use in cleaning silicon wafers)
IT 52622-80-7, Dioxol
(perfluoro-, tetrafluoroethylene resin contg., glass coating with; manuf. of acid-resistant fluororesin-coated quartz glass jig for use in cleaning silicon wafers)
IT 9002-84-0, Tetrafluoroethylene resin
(perfluoroalkyl vinyl ether derivs., glass coating with; manuf. of acid-resistant fluororesin-coated quartz glass jig for use in cleaning silicon wafers)
IT 7664-39-3, Hydrofluoric acid, processes
(pickling of silicon wafers by; manuf. of acid-resistant fluororesin-coated quartz glass jig for use in cleaning silicon wafers)
IT 60676-86-0, Silica, vitreous
(quartz glass jig; manuf. of acid-resistant fluororesin-coated quartz glass jig for use in cleaning silicon wafers)
IT 7440-21-3, Silicon, processes
(silicon wafers; manuf. of acid-resistant fluororesin-coated quartz glass jig for use in cleaning silicon wafers)
IT 12125-01-8, Ammonium fluoride
(soln. contg. HF and ammonium fluoride; manuf. of acid-resistant fluororesin-coated quartz glass jig for use in cleaning silicon wafers)

L16 ANSWER 2 OF 13 USPAT2 on STN
AN 2001:176432 USPAT2
TI Method and apparatus for separating semiconductor elements, and mounting method of semiconductor elements
IN Odajima, Hitoshi, Yokohama, JAPAN
Futagi, Kazuyuki, Yokohama, JAPAN
Matsuoka, Makoto, Hadano, JAPAN
PA Hitachi, Ltd., Tokyo, JAPAN (non-U.S. corporation)
PI US 6585471 B2 20030701
AI US 2001-877008 20010611 (9)
RLI Division of Ser. No. US 2000-516504, filed on 1 Mar 2000, now patented, Pat. No. US 6297075
PRAI JP 1999-56080 19990303
JP 1999-251248 19990830
DT Utility
FS GRANTED
EXNAM Primary Examiner: Bratlie, Steven A.
LREP Antonelli, Terry, Stout & Kraus, LLP
CLMN Number of Claims: 13
ECL Exemplary Claim: 1
DRWN 87 Drawing Figure(s); 29 Drawing Page(s)
LN.CNT 2096
AB A method and an apparatus wherein the thin semiconductor wafer is cut into a unit of a thin semiconductor element under the condition of being stuck on an adhesive sheet. A group of the semiconductor elements are removed from the adhesive sheet at high speed without incurring and breaking each semiconductor element thereof, and the semiconductor elements are picked up from the removed group of the semiconductor elements by a predetermined unit.
INCL INCLM: 414/403.000
INCLS: 156/344.000; 156/584.000
NCL NCLM: 414/403.000
NCLS: 156/344.000; 156/584.000
IC [7]

ICM: H05K013-02
EXF 156/584; 156/344; 414/403
ARTU 362

L16 ANSWER 3 OF 13 USPATFULL on STN
AN 2001:176432 USPATFULL
TI Method and apparatus for separating semiconductor elements, and mounting method of semiconductor elements
IN Odajima, Hitoshi, Yokohama, Japan
Futagi, Kazuyuki, Yokohama, Japan
Matsuoka, Makoto, Hadano, Japan
PI US 2001029088 A1 20011011
US 6585471 B2 20030701
AI US 2001-877008 A1 20010611 (9)
RLI Division of Ser. No. US 2000-516504, filed on 1 Mar 2000, PENDING
PRAI JP 1999-56080 19990303
JP 1999-251248 19990830
DT Utility
FS APPLICATION
LREP ANTONELLI TERRY STOUT AND KRAUS, SUITE 1800, 1300 NORTH SEVENTEENTH STREET, ARLINGTON, VA, 22209
CLMN Number of Claims: 27
ECL Exemplary Claim: 1
DRWN 29 Drawing Page(s)
LN.CNT 2304
AB For providing a method and an apparatus thereof, wherein a thin semiconductor wafer is cut out into a unit of a thin semiconductor element under the condition of being stuck on an adhesive sheet, a group of the semiconductor elements are removed from the adhesive sheet at high speed without injuring and breaking each semiconductor element thereof, and the semiconductor elements are picked up from the removed group of the semiconductor elements by a predetermined unit, according to the present invention, the separating method comprising: a separation step for holding on a chuck a group of semiconductor elements with positioning objects, being stuck on an adhesive sheet fixed on a frame at periphery thereof under condition of a semiconductor wafer and cut into a unit of a semiconductor element, for cutting the adhesive sheet around the group of semiconductor elements being held, and for striping the cut adhesive sheet from said group of semiconductor elements being held; and a storing step for storing into a tray, for picking up the semiconductor elements by a desired unit thereof from the group of semiconductor elements being stripped with the adhesive sheet in said separation step and held on the chuck, so as to store into a tray.
INCL INCLM: 438/464.000
INCLS: 438/465.000
NCL NCLM: 414/403.000
NCLS: 156/344.000; 156/584.000
IC [7]
ICM: H01L021-00
ICS: H01L021-78; H01L021-301; H01L021-46

L16 ANSWER 4 OF 13 USPATFULL on STN
AN 2001:176408 USPATFULL
TI Method and apparatus for separating semiconductor elements, and mounting method of semiconductor elements
IN Odajima, Hitoshi, Yokohama, Japan
Futagi, Kazuyuki, Yokohama, Japan
Matsuoka, Makoto, Hadano, Japan
PI US 2001029064 A1 20011011
US 6544819 B2 20030408
AI US 2001-877007 A1 20010611 (9)
RLI Continuation of Ser. No. US 2000-516504, filed on 1 Mar 2000, PENDING
PRAI JP 1999-56080 19990303
JP 1999-251248 19990830

DT Utility
FS APPLICATION
LREP ANTONELLI TERRY STOUT AND KRAUS, SUITE 1800, 1300 NORTH SEVENTEENTH STREET, ARLINGTON, VA, 22209
CLMN Number of Claims: 27
ECL Exemplary Claim: 1
DRWN 29 Drawing Page(s)
LN.CNT 2304
AB For providing a method and an apparatus thereof, wherein a thin semiconductor wafer is cut out into a unit of a thin semiconductor element under the condition of being stuck on an adhesive sheet, a group of the semiconductor elements are removed from the adhesive sheet at high speed without injuring and breaking each semiconductor element thereof, and the semiconductor elements are picked up from the removed group of the semiconductor elements by a predetermined unit, according to the present invention, the separating method comprising: a separation step for holding on a chuck a group of semiconductor elements with positioning objects, being stuck on an adhesive sheet fixed on a frame at periphery thereof under condition of a semiconductor wafer and cut into a unit of a semiconductor element, for cutting the adhesive sheet around the group of semiconductor elements being held, and for striping the cut adhesive sheet from said group of semiconductor elements being held; and a storing step for storing into a tray, for picking up the semiconductor elements by a desired unit thereof from the group of semiconductor elements being stripped with the adhesive sheet in said separation step and held on the chuck, so as to store into a tray.
INCL INCLM: 438/113.000
INCLS: 438/464.000; 438/465.000; 257/620.000
NCL NCLM: 438/118.000
NCLS: 438/106.000; 438/110.000; 438/460.000; 438/464.000
IC [7]
ICM: H01L021-44
ICS: H01L021-48; H01L021-50; H01L021-301; H01L021-46; H01L021-78; H01L023-544

L16 ANSWER 5 OF 13 USPATFULL on STN
AN 2001:167963 USPATFULL
TI Method and apparatus for separating semiconductor elements, and mounting method of semiconductor elements
IN Odajima, Hitoshi, Yokohama, Japan
Futagi, Kazuyuki, Yokohama, Japan
Matsuoka, Makoto, Hadano, Japan
PA Hitachi, Ltd., Tokyo, Japan (non-U.S. corporation)
PI US 6297075 B1 20011002
AI US 2000-516504 20000301 (9)
PRAI JP 1999-56080 19990303
JP 1999-251248 19990906
DT Utility
FS GRANTED
EXNAM Primary Examiner: Picardat, Kevin M.; Assistant Examiner: Collins, D. M.
LREP Antonelli, Terry, Stout & Kraus, LLP
CLMN Number of Claims: 7
ECL Exemplary Claim: 1
DRWN 87 Drawing Figure(s); 29 Drawing Page(s)
LN.CNT 2116
AB For providing a method and an apparatus thereof, wherein a thin semiconductor wafer is cut out into a unit of a thin semiconductor element under the condition of being stuck on an adhesive sheet, a group of the semiconductor elements are removed from the adhesive sheet at high speed without injuring and breaking each semiconductor element thereof, and the semiconductor elements are picked up from the removed group of the semiconductor elements by a predetermined unit, according to the present invention, the separating method comprising: a separation step for holding on a chuck a group of semiconductor elements with

positioning objects, being stuck on an adhesive sheet fixed on a frame at periphery thereof under condition of a semiconductor wafer and cut into a unit of a semiconductor element, for cutting the adhesive sheet around the group of semiconductor elements being held, and for striping the cut adhesive sheet from said group of semiconductor elements being held; and a storing step for storing into a tray, for picking up the semiconductor elements by a desired unit thereof from the group of semiconductor elements being stripped with the adhesive sheet in said separation step and held on the chuck, so as to store into a tray.

INCL INCLM: 438/110.000
INCLS: 438/118.000; 438/460.000; 438/464.000
NCL NCLM: 438/110.000
NCLS: 438/118.000; 438/460.000; 438/464.000
IC [7]
ICM: H01L021-44
ICS: H01L021-48; H01L021-50
EXF 438/106; 438/118; 438/110; 438/460; 438/464
ARTU 283

L16 ANSWER 6 OF 13 USPAT2 on STN
AN 2001:176408 USPAT2
TI Method and apparatus for separating semiconductor elements, and mounting method of semiconductor elements
IN Odajima, Hitoshi, Yokohama, JAPAN
Futagi, Kazuyuki, Yokohama, JAPAN
Matsuoka, Makoto, Hadano, JAPAN
PA Hitachi, Ltd., Tokyo, JAPAN (non-U.S. corporation)
PI US 6544819 B2 20030408
AI US 2001-877007 20010611 (9)
RLI Continuation of Ser. No. US 2000-516504, filed on 1 Mar 2000, now patented, Pat. No. US 6297075
PRAI JP 1999-56080 19990303
JP 1999-251248 19990830
DT Utility
FS GRANTED
EXNAM Primary Examiner: Coleman, William David; Assistant Examiner: Collins, D. M.
LREP Antonelli, Terry, Stout & Kraus, LLP
CLMN Number of Claims: 4
ECL Exemplary Claim: 1
DRWN 87 Drawing Figure(s); 29 Drawing Page(s)
LN.CNT 2087
AB A method and an apparatus wherein the thin semiconductor wafer is cut into a unit of a thin semiconductor element under the condition of being stuck on an adhesive sheet. A group of the semiconductor elements are removed from the adhesive sheet at high speed without incurring and breaking each semiconductor element thereof, and the semiconductor elements are picked up from the removed group of the semiconductor elements by a predetermined unit.
INCL INCLM: 438/118.000
INCLS: 438/106.000; 438/110.000; 438/460.000; 438/464.000
NCL NCLM: 438/118.000
NCLS: 438/106.000; 438/110.000; 438/460.000; 438/464.000
IC [7]
ICM: H01L021-44
ICS: H01L021-48; H01L021-50
EXF 438/118; 438/106; 438/110; 438/460; 438/464
ARTU 283

L16 ANSWER 7 OF 13 USPATFULL on STN
AN 2002:164163 USPATFULL
TI Rolling bearing and rolling bearing device
IN Shoda, Yoshio, Kanagawa, JAPAN
Liu, Jun, Kanagawa, JAPAN

Sato, Yukio, Kanagawa, JAPAN
PA NSK LTD. (non-U.S. corporation)
PI US 2002085773 A1 20020704
US 6575631 B2 20030610
AI US 2001-970804 A1 20011005 (9)
RLI Continuation-in-part of Ser. No. US 2000-584130, filed on 31 May 2000, GRANTED, Pat. No. US 6382836
PRAI JP 1999-152757 19990531
JP 2000-305929 20001005
JP 2000-323086 20001023
JP 2000-323206 20001023
JP 2000-403102 20001228
JP 2001-90814 20010327
JP 2001-180535 20010614
JP 2001-294399 20010926
DT Utility
FS APPLICATION
LREP SUGHRUE, MION, ZINN,, MACPEAK & SEAS, PLLC, 2100 Pennsylvania Avenue, NW, Washington, DC, 20037-3213
CLMN Number of Claims: 23
ECL Exemplary Claim: 1
DRWN 77 Drawing Page(s)
LN.CNT 3759
AB Into a raceway groove formed between outer and inner races, there are incorporated a plurality of rolling elements of which outside diameters serving as the rolling contact surfaces thereof each has a curvature in the axial direction as well and also each of which has a radius smaller than the radius of the raceway surfaces of the outer and inner races. The rolling elements are arranged in such a manner that the mutually adjoining rolling elements cross each other alternately and also that the outside diameters of the respective rolling elements are always contacted at two points with the raceway surfaces of one race and the raceway surfaces of the other race.
INCL INCLM: 384/047.000
NCL NCLM: 384/047.000
NCLS: 384/447.000; 384/619.000
IC [7]
ICM: A47C001-00

L16 ANSWER 8 OF 13 USPAT2 on STN
AN 2002:164163 USPAT2
TI Rolling bearing and rolling bearing device
IN Shoda, Yoshio, Kanagawa, JAPAN
Liu, Jun, Kanagawa, JAPAN
Sato, Yukio, Kanagawa, JAPAN
PA NSK Ltd., Tokyo, JAPAN (non-U.S. corporation)
PI US 6575631 B2 20030610
AI US 2001-970804 20011005 (9)
RLI Continuation-in-part of Ser. No. US 2000-584130, filed on 31 May 2000
PRAI JP 1999-152757 19990531
JP 2000-305929 20001005
JP 2000-323086 20001023
JP 2000-323206 20001023
JP 2000-403102 20001228
JP 2001-90814 20010327
JP 2001-180535 20010614
JP 2001-294399 20010926
DT Utility
FS GRANTED
EXNAM Primary Examiner: Footland, Lenard A.
LREP Sughrue Mion, PLLC
CLMN Number of Claims: 28
ECL Exemplary Claim: 1
DRWN 104 Drawing Figure(s); 77 Drawing Page(s)

LN.CNT 3691
AB Into a raceway groove formed between outer and inner races, there are incorporated a plurality of rolling elements of which outside diameters serving as the rolling contact surfaces thereof each has a curvature in the axial direction as well and also each of which has a radius smaller than the radius of the raceway surfaces of the outer and inner races. The rolling elements are arranged in such a manner that the mutually adjoining rolling elements cross each other alternately and also that the outside diameters of the respective rolling elements are always contacted at two points with the raceway surfaces of one race and the raceway surfaces of the other race.
INCL INCLM: 384/047.000
INCLS: 384/447.000; 384/619.000
NCL NCLM: 384/047.000
NCLS: 384/447.000; 384/619.000
IC [7]
ICM: F16C029-04
EXF 384/47; 384/447; 384/619; 384/51; 384/50
ARTU 362

L16 ANSWER 9 OF 13 USPATFULL on STN
AN 2001:149505 USPATFULL
TI Method of producing semiconductor thin film and method of producing solar cell using same
IN Mizutani, Masaki, Isehara-shi, Japan
Tanikawa, Isao, Hiratsuka-shi, Japan
Nakagawa, Katsumi, Atsugi-shi, Japan
Shoji, Tatsumi, Hiratsuka-shi, Japan
Ukiyo, Noritaka, Atsugi-shi, Japan
Iwasaki, Yukiko, Atsugi-shi, Japan
PI US 2001018949 A1 20010906
AI US 2001-813137 A1 20010321 (9)
RLI Division of Ser. No. US 1999-333019, filed on 15 Jun 1999, GRANTED, Pat. No. US 6258666
PRAI JP 1998-171403 19980618
JP 1999-159374 19990607
DT Utility
FS APPLICATION
LREP FITZPATRICK CELLA HARPER & SCINTO, 30 ROCKEFELLER PLAZA, NEW YORK, NY, 10112
CLMN Number of Claims: 29
ECL Exemplary Claim: 1
DRWN 7 Drawing Page(s)
LN.CNT 564
CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AB Provided is a method of producing a semiconductor thin film wherein while a semiconductor thin film formed on a substrate is supported on a curved surface of a support member having the curved surface, the support member is rotated, thereby peeling the semiconductor thin film away from the substrate. Also provided is a method of producing a semiconductor thin film having the step of peeling a semiconductor thin film formed on a substrate away from the substrate, wherein the peeling step is carried out after the substrate is secured on a substrate support member without an adhesive. These provide the method of peeling the semiconductor thin film away from the substrate without damage and the method of holding the substrate without contamination.
INCL INCLM: 156/233.000
INCLS: 156/249.000
NCL NCLM: 156/233.000
NCLS: 156/249.000
IC [7]
ICM: B44C001-00
ICS: C09J001-00

CHEMICAL ABSTRACTS INDEXING COPYRIGHT 2003 ACS on STN

	PATENT	KIND	DATE
OS CA 132:52381 *	EP 965664	A1	19991222

* CA Indexing for this record included
CC 52-2 (Electrochemical, Radiational, and Thermal Energy Technology)
ST solar cell semiconductor thin film prepn
IT Adhesives
(conductive; method of producing semiconductor thin film and solar cell)
IT Epitaxy
Semiconductor films
Solar cells
(method of producing semiconductor thin film and solar cell)
IT 24937-78-8, Eva 25038-71-5, Ethylene-tetrafluoroethylene copolymer
(light-transmitting film; method of producing semiconductor thin film and solar cell)
IT 7440-21-3, Silicon, uses
(method of producing semiconductor thin film and solar cell)
IT 7429-90-5, Aluminum, uses
(substrate; method of producing semiconductor thin film and solar cell)

L16 ANSWER 10 OF 13 USPATFULL on STN
AN 2001:107750 USPATFULL
TI Method of producing semiconductor thin film and method of producing solar cell using same
IN Mizutani, Masaki, Isehara, Japan
Tanikawa, Isao, Hiratsuka, Japan
Nakagawa, Katsumi, Atsugi, Japan
Shoji, Tatsumi, Hiratsuka, Japan
Ukiyo, Noritaka, Atsugi, Japan
Iwasaki, Yukiko, Atsugi, Japan
PA Canon Kabushiki Kaisha, Tokyo, Japan (non-U.S. corporation)
PI US 6258666 B1 20010710
AI US 1999-333019 19990615 (9)
PRAI JP 1998-171403 19980618
JP 1999-159374 19990607
DT Utility
FS GRANTED
EXNAM Primary Examiner: Chaudhuri, Olik; Assistant Examiner: Rao, Shrinivas H.
LREP Fitzpatrick, Cella, Harper & Scinto
CLMN Number of Claims: 22
ECL Exemplary Claim: 1
DRWN 18 Drawing Figure(s); 7 Drawing Page(s)
LN.CNT 505
CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AB Provided is a method of producing a semiconductor thin film wherein while a semiconductor thin film formed on a substrate is supported on a curved surface of a support member having the curved surface, the support member is rotated, thereby peeling the semiconductor thin film away from the substrate. Also provided is a method of producing a semiconductor thin film having the step of peeling a semiconductor thin film formed on a substrate away from the substrate, wherein the peeling step is carried out after the substrate is secured on a substrate support member without an adhesive. These provide the method of peeling the semiconductor thin film away from the substrate without damage and the method of holding the substrate without contamination.
INCL INCLM: 438/258.000
INCLS: 438/255.000; 156/241.000; 156/247.000; 226/096.000
NCL NCLM: 438/258.000
NCLS: 156/241.000; 156/247.000; 226/096.000; 257/E21.567; 438/255.000
IC [7]
ICM: H01L021-336

ICS: H01L021-8242; B44C021-8242; B32B031-00; B65H020-00
EXF 438/458; 438/71; 438/455; 479/98; 136/255; 136/256; 136/261; 225/464; 225/975; 205/255; 205/256; 205/261; 117/43; 117/44; 117/45; 117/915
ARTU 284

CHEMICAL ABSTRACTS INDEXING COPYRIGHT 2003 ACS on STN

	PATENT	KIND	DATE
OS CA 132:52381 *	EP 965664	A1	19991222

* CA Indexing for this record included
CC 52-2 (Electrochemical, Radiational, and Thermal Energy Technology)
ST solar cell semiconductor thin film prepn
IT Adhesives
(conductive; method of producing semiconductor thin film and solar cell)
IT Epitaxy
Semiconductor films
Solar cells
(method of producing semiconductor thin film and solar cell)
IT 24937-78-8, Eva 25038-71-5, Ethylene-tetrafluoroethylene copolymer
(light-transmitting film; method of producing semiconductor thin film and solar cell)
IT 7440-21-3, Silicon, uses
(method of producing semiconductor thin film and solar cell)
IT 7429-90-5, Aluminum, uses
(substrate; method of producing semiconductor thin film and solar cell)

L16 ANSWER 11 OF 13 USPATFULL on STN
AN 78:11250 USPATFULL
TI Fiber-optic device with curved sleeve and filler matrix
IN Moraschetti, Nando, Bergdietikon, Switzerland
PA Volpi AG, Urdorf, Switzerland (non-U.S. corporation)
PI US 4076377 19780228
AI US 1976-655572 19760205 (5)
PRAI CH 1975-2091 19750219
DT Utility
FS Granted
EXNAM Primary Examiner: Rubin, David H.
LREP Toren, McGeady and Stanger
CLMN Number of Claims: 9
ECL Exemplary Claim: 9
DRWN 2 Drawing Figure(s); 1 Drawing Page(s)
LN.CNT 476
AB A generally flexible fiber-optic light guide comprising a multifilament bundle of coated fibers in a sheath and having at least one permanently bent portion defining a rigid curve, the bent portion being arranged within an end piece or socket of the light guide; the coated fibers within the bent portion being closely packed and embedded in a solid material capable of serving as a lubricant when in an uncured state. The permanently bent portion is produced by arranging the coated fiber closely packed in a straight tube made of a ductile material, filling the tube with an agent capable of serving as a lubricating agent when in an uncured state, bending said tube with the fibers and the lubricating agent and curing the lubricating agent so as to form a solid matrix or bedding for the fibers in the bent portion.
INCL INCLM: 350/096.250
NCL NCLM: 385/116.000
IC [2]
ICM: G02B005-16
EXF 350/96B; 350/96BC; 350/96C
ARTU 257

L16 ANSWER 12 OF 13 USPATFULL on STN

AN 2001:185192 USPATFULL
TI Method for production of semiconductor device
IN Hasunuma, Masahiko, Yokohama, Japan
Ito, Sachiyo, Yokohama, Japan
Shimamura, Keizo, Kawasaki, Japan
Kaneko, Hisashi, Fujisawa, Japan
Hayasaka, Nobuo, Yokosuka, Japan
Tsutsumi, Junsei, Kawasaki, Japan
Kajita, Akihiro, Yokohama, Japan
Wada, Junichi, Yokohama, Japan
Okano, Haruo, Chiba-ken, Japan
PA Kabushiki Kaisha Toshiba, Kawasaki, Japan (non-U.S. corporation)
PI US 6306756 B1 20011023
AI US 2000-580922 20000526 (9)
RLI Division of Ser. No. US 1995-521088, filed on 20 Jun 1995, now patented, Pat. No. US 6090701
PRAI JP 1994-162801 19940621
JP 1995-79749 19950310
DT Utility
FS GRANTED
EXNAM Primary Examiner: Quach, T. N.
LREP Finnegan, Henderson, Farabow, Garrett & Dunner, L.L.P.
CLMN Number of Claims: 10
ECL Exemplary Claim: 1
DRWN 68 Drawing Figure(s); 21 Drawing Page(s)
LN.CNT 3071
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AB A method for the production of a semiconductor device having an electrode line formed in a semiconducting substrate is disclosed which comprises preparing a semiconducting substrate having trenches and/or contact holes formed preparatorily in a region destined to form the electrode line, forming a conductive film formed mainly of at least one member selected from among Cu, Ag, and Au on the surface of the semiconducting substrate, heat-treating the superposed Cu film while supplying at least an oxidizing gas thereto thereby flowing the Cu film and causing never melting to fill the trenches and/or contact holes, and removing by polishing the part of the conductive film which falls outside the region of the electrode line and completing the electrode lines consequently. During the heat treatment, a reducing gas is supplied in addition to the oxidizing gas to induce a local oxidation-reduction reaction and fluidify and/or flow the conductive film and consequently accomplish the embodiment of the conductive film in the trenches. The formation of the interconnection is also accomplished by forming a conductive film on the surface of a semiconducting substrate having trenches formed therein, exerting thereon uniaxial stress from above the semiconducting substrate, heat treating the formed conductive film thereby flowing the conductive film, to fill the trenches, and polishing the surface of the semiconducting substrate.

INCL INCLM: 438/632.000
INCLS: 438/646.000; 438/650.000; 438/687.000
NCL NCLM: 438/632.000
NCLS: 257/E21.588; 438/646.000; 438/650.000; 438/687.000
IC [7]
ICM: H01L021-4763
EXF 438/632; 438/633; 438/646; 438/650; 438/687
ARTU 284

CHEMICAL ABSTRACTS INDEXING COPYRIGHT 2003 ACS on STN

	PATENT	KIND	DATE
OS CA 126:151582 *	JP 08316233	A2	19961129

* CA Indexing for this record included

CC 76-3 (Electric Phenomena)
ST copper interconnection reflow semiconductor device; silver interconnection reflow semiconductor device; gold interconnection reflow semiconductor device
IT Interconnections (electric)
Semiconductor devices
(manuf. of semiconductor devices with reliable electrode interconnections by reflow process)
IT 7440-22-4, Silver, processes
(manuf. of semiconductor devices with reliable electrode interconnections)
IT 7440-50-8, Copper, processes 7440-57-5, Gold, processes
(manuf. of semiconductor devices with reliable electrode interconnections by reflow process)

L16 ANSWER 13 OF 13 USPATFULL on STN
AN 2000:91856 USPATFULL
TI Method for production of semiconductor device
IN Hasunuma, Masahiko, Yokohama, Japan
Ito, Sachiyo, Yokohama, Japan
Shimamura, Keizo, Kawasaki, Japan
Kaneko, Hisashi, Fujisawa, Japan
Hayasaka, Nobuo, Yokosuka, Japan
Tsutsumi, Junsei, Kawasaki, Japan
Kajita, Akihiro, Yokohama, Japan
Wada, Junichi, Yokohama, Japan
Okano, Haruo, Chiba-ken, Japan
PA Kabushiki Kaisha Toshiba, Kawasaki, Japan (non-U.S. corporation)
PI US 6090701 20000718
AI US 1995-521088 19950620 (8)
PRAI JP 1994-162801 19940621
JP 1995-79749 19950310
DT Utility
FS Granted
EXNAM Primary Examiner: Quach, T. N.
LREP Finnegan, Henderson, Farabow, Garrett & Dunner, L.L.P.
CLMN Number of Claims: 11
ECL Exemplary Claim: 1
DRWN 68 Drawing Figure(s); 21 Drawing Page(s)
LN.CNT 3158
CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AB A method for the production of a semiconductor device having an electrode line formed in a semiconducting substrate is disclosed which comprises preparing a semiconducting substrate having trenches and/or contact holes formed preparatorily in a region destined to form the electrode line, forming a conductive film formed mainly of at least one member selected from among Cu, Ag, and Au on the surface of the semiconducting substrate, heat-treating the superposed Cu film while supplying at least an oxidizing gas thereto thereby flowing the Cu film to fill the trenches and/or contact holes, and removing by polishing the part of the conductive film which falls outside the region of the electrode line and completing the electrode lines consequently. During the heat treatment, a reducing gas is supplied in addition to the oxidizing gas to induce a local oxidation-reduction reaction and fluidify and/or flow the conductive film and consequently accomplish the embodiment of the conductive film in the trenches.
INCL INCLM: 438/632.000
INCLS: 438/633.000; 438/646.000; 438/650.000; 438/687.000
NCL NCLM: 438/632.000
NCLS: 257/E21.588; 438/633.000; 438/646.000; 438/650.000; 438/687.000
IC [7]
ICM: H01L021-4763
EXF 437/187; 437/188; 437/189; 437/190; 437/192; 437/201; 437/173; 437/174; 438/632; 438/646; 438/650; 438/627; 438/686; 438/687; 438/626; 438/629;

438/633; 438/631
ARTU 284

CHEMICAL ABSTRACTS INDEXING COPYRIGHT 2003 ACS on STN

	PATENT	KIND	DATE
OS CA 126:151582 *	JP 08316233	A2	19961129

* CA Indexing for this record included
CC 76-3 (Electric Phenomena)
ST copper interconnection reflow semiconductor device; silver interconnection reflow semiconductor device; gold interconnection reflow semiconductor device
IT Interconnections (electric)
Semiconductor devices
(manuf. of semiconductor devices with reliable electrode interconnections by reflow process)
IT 7440-22-4, Silver, processes
(manuf. of semiconductor devices with reliable electrode interconnections)
IT 7440-50-8, Copper, processes 7440-57-5, Gold, processes
(manuf. of semiconductor devices with reliable electrode interconnections by reflow process)

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L16 ANSWER 1 OF 3 CAPLUS COPYRIGHT 2003 ACS on STN
AN 2002:446111 CAPLUS
DN 137:9680
TI Manufacture of acid-resistant fluororesin-coated quartz glass jig for use in cleaning silicon wafers
IN Inaki, Kyoichi; Araki, Ifsuo
PA Heraeus Quarzglas Gmbh & Co. Kg, Germany; Shin-Etsu Quartz Products Co., Ltd.
SO Eur. Pat. Appl., 6 pp.
CODEN: EPXXDW
DT Patent
LA English
IC ICM C03C017-32
CC 57-1 (Ceramics)
Section cross-reference(s): 76
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI EP 1213269	A1	20020612	EP 2001-128581	20011130 <--
R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO, MK, CY, AL, TR				
JP 2002176023	A2	20020621	JP 2000-369534	20001205 <--
US 2002106518	A1	20020808	US 2001-6827	20011204 <--
PRAI JP 2000-369534	A	20001205 <--		

AB The fluororesin-coated quartz glass jig is free from the coating peeling off by attacking hydrofluoric acid or from generating particles due to the etching of quartz glass, while yet preventing the generation of chipping by relaxing the impact imposed on the quartz glass by silicon wafers. The surface of the quartz glass jig is wholly covered with a pinhole-free fluororesin coating .gtoreq.50 .mu.m thick. The fluororesin is selected from tetrafluoroethylene resin, tetrafluoroethyleneperfluoroalkyl vinyl ether resin, perfluoroethylenepropylene resin, ethylenetetrafluoroethylene resin, chlorotrifluoroethylene resin, ethylenechlorotrifluoroethylene resin, vinylidene difluoride resin, vinyl fluoride resin, and tetrafluoroethyleneperfluorodioxol resin.
ST quartz glass silicon wafer cleaning fluororesin coating; semiconductor device fabrication silicon wafer cleaning
IT Coating materials
(acid-resistant; manuf. of acid-resistant fluororesin-coated quartz glass jig for use in cleaning silicon wafers)
IT Semiconductor device fabrication
(cleaning silicon wafers; manuf. of acid-resistant fluororesin-coated quartz glass jig for use in cleaning silicon wafers)
IT Fluoropolymers, uses
RL: TEM (Technical or engineered material use); USES (Uses)
(fluororesin coating; manuf. of acid-resistant fluororesin-coated quartz glass jig for use in cleaning silicon wafers)
IT Etching
(of quartz glass; manuf. of acid-resistant fluororesin-coated quartz glass jig for use in cleaning silicon wafers)
IT Fluoropolymers, uses
RL: TEM (Technical or engineered material use); USES (Uses)
(perfluoroalkyl vinyl ether derivs., glass coating with; manuf. of acid-resistant fluororesin-coated quartz glass jig for use in cleaning silicon wafers)
IT 7631-86-9, Silicon dioxide, uses
RL: TEM (Technical or engineered material use); USES (Uses)
(cryst. powder; manuf. of acid-resistant fluororesin-coated quartz glass jig for use in cleaning silicon wafers)
IT 75-02-5D, Vinyl fluoride, resin 75-38-7D, Vinylidene difluoride, resin 79-38-9D, Chlorotrifluoroethylene, resin 25038-71-5, Ethylenetetrafluoroethylene copolymer 25101-45-5, Ethylenechlorotrifluoroethylene copolymer 27029-05-6,

Perfluoroethylenepropylene copolymer
RL: TEM (Technical or engineered material use); USES (Uses)
(glass coating with; manuf. of acid-resistant fluororesin-coated quartz glass jig for use in cleaning silicon wafers)
IT 52622-80-7, Dioxol
RL: TEM (Technical or engineered material use); USES (Uses)
(perfluoro-, tetrafluoroethylene resin contg., glass coating with; manuf. of acid-resistant fluororesin-coated quartz glass jig for use in cleaning silicon wafers)
IT 9002-84-0, Tetrafluoroethylene resin
RL: TEM (Technical or engineered material use); USES (Uses)
(perfluoroalkyl vinyl ether derivs., glass coating with; manuf. of acid-resistant fluororesin-coated quartz glass jig for use in cleaning silicon wafers)
IT 7664-39-3, Hydrofluoric acid, processes
RL: PEP (Physical, engineering or chemical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(pickling of silicon wafers by; manuf. of acid-resistant fluororesin-coated quartz glass jig for use in cleaning silicon wafers)
IT 60676-86-0, Silica, vitreous
RL: DEV (Device component use); TEM (Technical or engineered material use); USES (Uses)
(quartz glass jig; manuf. of acid-resistant fluororesin-coated quartz glass jig for use in cleaning silicon wafers)
IT 7440-21-3, Silicon, processes
RL: PEP (Physical, engineering or chemical process); PYP (Physical process); TEM (Technical or engineered material use); PROC (Process); USES (Uses)
(silicon wafers; manuf. of acid-resistant fluororesin-coated quartz glass jig for use in cleaning silicon wafers)
IT 12125-01-8, Ammonium fluoride
RL: MOA (Modifier or additive use); USES (Uses)
(soln. contg. HF and ammonium fluoride; manuf. of acid-resistant fluororesin-coated quartz glass jig for use in cleaning silicon wafers)
RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
RE
(1) Anon; PATENT ABSTRACTS OF JAPAN 1985, V009(288), PE-358
(2) Anon; PATENT ABSTRACTS OF JAPAN 1995, V1995(07)
(3) Anon; PATENT ABSTRACTS OF JAPAN 1998, V1998(06)
(4) Heraeus, Q; WO 0032529 A 2000 CAPLUS
(5) Shinetsu Quartz Prod Co Ltd; JP 10036140 A 1998 CAPLUS
(6) Toho Kasei Kk; JP 07089603 A 1995
(7) Toshiba Kk; JP 60128623 A 1985
(8) Univ Utrecht; WO 8706927 A 1987 CAPLUS
RN 7631-86-9
RN 75-02-5D
RN 75-38-7D
RN 79-38-9D
RN 25038-71-5
RN 25101-45-5
RN 27029-05-6
RN 52622-80-7
RN 9002-84-0
RN 7664-39-3
RN 60676-86-0
RN 7440-21-3
RN 12125-01-8

L16 ANSWER 2 OF 3 WPIDS COPYRIGHT 2003 THOMSON DERWENT on STN
AN 2002-683955 [74] WPIDS
DNN N2002-539958 DNC C2002-193212
TI Fluororesin-coated quartz glass jig e.g. wafer carrier boats for use in cleaning silicon wafers, has surface entirely covered with a pinhole-free fluororesin coating.

DC A14 A88 L01 L03 P73 U11
IN ARAKI, I; INAKI, K
PA (HERA) HERAEUS QUARZGLAS GMBH & CO KG; (SHIN-N) SHINETSU QUARTZ PROD CO LTD; (SHIN-N) SHINETSU SEKIEI KK; (ARAK-I) ARAKI I; (INAK-I) INAKI K
CYC 28
PI EP 1213269 A1 20020612 (200274)* EN 6p C03C017-32
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR
JP 2002176023 A 20020621 (200274) 4p H01L021-304
US 2002106518 A1 20020808 (200274) B32B027-00
ADT EP 1213269 A1 EP 2001-128581 20011130; JP 2002176023 A **JP 2000-369534 20001205**; US 2002106518 A1 US 2001-6827 20011204
PRAI **JP 2000-369534 20001205**
IC ICM B32B027-00; C03C017-32; H01L021-304
AB EP 1213269 A UPAB: 20021118
NOVELTY - The entire surface of fluororesin-coated quartz glass jig is covered with a pinhole free fluororesin coating.
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for producing fluororesin-coated quartz glass jig, involves rounding all the edges of jig into curved portions each having a curvature (r) of 0.5 mm or more, and treating the resulting jig with fluororesin coating agent to form fluororesin coating on entire quartz glass jig.
USE - For e.g. wafer carrier boats and chucks, for use in cleaning silicon wafers.
ADVANTAGE - Since pinhole-free fluororesin is coated on entire surface of quartz glass jig, direct contact of quartz glass jig with hydrochloric acid solution is prevented. Thus, peeling of fluororesin coating or generation of particles during etching of quartz glass are prevented, while relaxing the impact on quartz glass imposed by silicon wafers, thereby preventing generation of chipping. The adhesiveness of fluororesin coating to quartz glass is improved by applying fluororesin solution having excellent heat resistance, chemical resistance, corrosion resistance and wear resistance, after subjecting quartz glass surface to frost treatment. By performing frost treatment, the irregularities are formed on surface of quartz glass and anchoring effect provided by the irregularities decreases peeling of film by improving adhesiveness of fluororesin coating. The silicon wafers are produced in high yield.
Dwg.0/0
FS CPI EPI GMPI
FA AB
MC CPI: A04-E10; A12-H; L01-G04B; L04-C09; L04-D
EPI: U11-C06A1B; U11-F02A2

L16 ANSWER 3 OF 3 JAPIO (C) 2003 JPO on STN
AN 2002-176023 JAPIO
TI FLUORORESIN-COATED QUARTZ GLASS JIG AND ITS MANUFACTURING METHOD
IN INAGI KYOICHI; ARAKI ITSUO
PA SHINETSU QUARTZ PROD CO LTD
PI JP 2002176023 A 20020621 Heisei
AI **JP 2000-369534** (JP2000369534 Heisei) 20001205
PRAI **JP 2000-36953420001205**
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2002
IC ICM H01L021-304
ICS C03C017-32
AB PROBLEM TO BE SOLVED: To provide a fluororesin-coated quartz glass jig the fluororesin coating film of which does not cause peeling due to hydrofluoric acid and the quartz glass of which does not produce particles even when the glass is etched and, in addition, does not cause chipping even when the jig is brought into collision with a silicon wafer, because the impact between the wafer and quartz glass is relieve.
SOLUTION: The whole surface of the fluororesin-coated quartz glass jig is covered with the pinhole-free fluororesin coating film. The method is used for manufacturing the jig.